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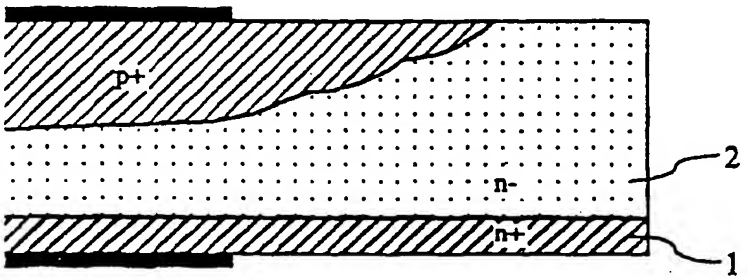
(54) Title: SiC SEMICONDUCTOR DEVICE COMPRISING A PN JUNCTION WITH A VOLTAGE ABSORBING EDGE

(57) Abstract

A semiconductor component, which comprises a pn junction, where both the p-conducting and the n-conducting layers of the pn junction constitute doped silicon carbide layers and where the edge of at least one of the conducting layers of the pn junction, exhibits a stepwise or uniformly decreasing total charge or effective surface charge density from the initial value at the defined working junction to a zero or almost zero total charge at the outermost edge of the junction following a radial direction from the central part of the junction towards the outermost edge.



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SiC semiconductor device comprising a pn junction with a voltage absorbing edge

TECHNICAL FIELD

The invention is relates to a semiconductor component with Silicon Carbide as base material, where the component comprises at least one pn junction and where a risk of voltage breakdown due to a strong electrical field at the edge of the junction is reduced as the pn junction displays an edge termination with a decreasing doping towards the edge of at least one of the semiconducting layers of the pn junction.

BACKGROUND ART

Semiconductor components based on Silicon Carbide as base material are continuously developed to be used in connection with high temperatures, high power applications and under high radiation conditions. Under such circumstances conventional semiconductors do not work satisfactorily. Evaluations indicate that SiC semiconductors of power MOSFET-type and diode rectifiers based on SiC would be able to operate over a greater voltage and temperature interval, e.g. up to 650 - 800 °C, and show better breaker properties such as lower losses and higher working frequencies and nevertheless have a volume 20 times smaller than corresponding Silicon components. These possible improvements are based on the favourable material properties that Silicon Carbide possesses in relation to Silicon, such e.g. a higher breakdown field (up to 10 times higher than Silicon), a higher thermal conductivity (more than 3 times higher than Silicon) and a higher energy band gap (2.9 eV for 6H-SiC, one of the crystal structures of SiC).

As SiC semiconductor technology is relatively young and in many aspects non-optimized, there are many critical manufacturing problems that are to be solved until SiC semiconductor devices may be realized experimentally and manufacturing in a great number may become a reality. This is especially

true for components intended for use in high-power and high-voltage applications.

One of the difficulties to overcome when manufacturing high voltage diodes or other types of semiconductor components comprising a voltage absorbing pn junction is to produce a proper junction termination at the edge of the junction. The electric field across the pn junction is very high, when a reverse voltage is applied across the pn junction.

A high reverse bias generating a strong electric field at the edge of the pn junction implies a great risk of voltage breakdown or flash-over at the edge of the junction. In the region of the component surface, where the pn junction reaches the surface, an increase of the electric field arises compared with the conditions existing within the bulk of the junction. This is due to the changeover from more homogeneous conditions inside the crystal of the component to the abrupt step out of the crystal lattice at the surface. This effect makes it very important to reduce the field concentration, where the junction reaches the surface. Combined with efforts to passivate the surface of the component, measures are taken to flatten out the electric field at the surface e.g. by acting on how the pn junction emerges at the surface. As an example it is known from Silicon power components to lap (grind or saw) the surface of the edge to a certain angle in relation to the pn junction to thereby flatten out the field. Another known technique is to gradually decrease the doping of the conducting area around the junction, such that the doping is reduced towards the outermost edge of the junction (so called Junction Termination Extension, JTE) in order to elimininate field concentration at the edge of the junction. These methods, known from Silicon technique, are difficult to apply to components based on Sicilcon Carbide due to the very hard material, doping through diffusion is extremely difficult and so on.

The above-mentioned problems have not been solved for pn junctions in SiC. Many of the problems to be solved when developing semiconductor components from SiC are reminiscent of those prevalent at the beginning of the corresponding Silicon components. Yet, the same techniques as those applicable to Silicon cannot be utilized when solving the specific problems related to production of SiC semiconductor components. As an example, doping through diffusion is not feasible for SiC, as diffusion coefficients are negligable below 2270 °K. Also, ion implantation of doping elements, a common technique when manufacturing SiC components, is difficult to master and not fully developed for SiC.

High voltage diodes from 6H-SiC with epitaxially formed pn junctions and Schottky junctions have been done experimentally (see e.g. M. Bhatnagar and B. J. Baliga, IEEE Trans. Electron Devices, vol. 40, no. 3 pp 645 - 655, March 1993 or P. G. Neudeck, D. J. Larkin, J. A. Powell, L. G. Matus and C. S. Salupo, Appl. Phys. Lett. vol 64, No 11, 14 March 1994, pp 1386-1388). Some of the problems related to SiC devices have thus been solved, but nothing is discussed about the problems connected to electric field concentration at the edges of the junction.

The electric field may be reduced at the edge of the pn junction by applying a semi-isolating layer to the edge of the junction of a SiC component. Such a solution is described in document PCT/SE94/00482.

Any method or device to accomplish a semiconductor component corresponding to the principle of Junction Termination Extension at a pn junction composed of Si is not known for a component, where SiC constitutes the base material of the junction. This invention aims at describing a voltage absorbing edge at a pn junction with a structure similar to JTE of a Si component.

The term SiC is used in the following text to refer to any of the principal crystal polytypes of this material known as 6H, 4H, 2H, 3C and 15R.

DESCRIPTION OF THE INVENTION

The invention is composed of a semiconductor component, which comprises a pn junction, where both the p-conducting and the n-conducting layers of the pn junction constitute doped silicon carbide layers and where the edge of at least one of the conducting layers of the pn junction, exhibits a stepwise or uniformly decreasing total charge or effective surface charge density from the initial value at the defined working junction to a zero or almost zero total charge at the outermost edge of the junction following a radial direction from the central part of the junction towards the outermost edge.

The invention further comprises methods for producing said SiC semiconductor component with a decreasing charge profile.

By manufacturing a SiC semiconductor component with the features described, the concentration of the electric field, when a high reverse voltage is applied to the pn junction, is eliminated as the electrical field is flattened out along the extended edge termination. Hence, the risk of a voltage breakdown at the edge of the junction before a breakdown somewhere in the defined working area of the junction is reduced. By forming the edges of a pn junction of SiC material with a structure similar to a Junction Termination Extension (JTE) of prior art silicon devices as described according to the invention, the reverse voltage over the junction may be considerably increased (3 times and more) before a breakdown occurs.

Furthermore the reliability and long term stability are improved. This is due to the reduction of the electric field in the SiC material at the periphery of the junction. At the

same time the maximum surface electric fieldmust be reduced by at least one order of magnitude. This relieves the stress inflicted on the passivation and isolation of the junction inflicted

The SiC semiconductor component is manufactured according to the invention by means of one of the alternative methods described below which have in common that the junction has decreasing total charge concentration towards the outer edge.

One way, method A, of achieving the component according to the invention is arrived at by starting with a silicon carbon wafer comprising of a doped layer of a first conducting type. On the wafer, at least two doped layers of a second conducting type are epitaxially grown, where the doping dose of each new second conducting type layer is successively increased. By means of masking and etching the layers of the second conducting type are then formed to have different extending areas, in that the layer closest to the wafer has the greatest extension, while consecutive layers of the second conductive type of successively higher doses are formed with consecutively decreasing areal extension. In the most simple embodiment only two doped layers of the second conducting type are grown and formed, a first layer with a lower dose closest to the wafer and a second layer with a higher dopant dose on top of the first layer. The etching is then performed in two steps, whereby the first layer is formed to have a greater areal extension than the second layer.

As an alternative manufacturing method, A2, the second layer of the second conducting type is accomplished by implantation of ions (e.g. Al or B for p-type, N for N-type) with the same type of charge carriers as in the first layer, in that an implanted second layer with a higher dose and a lesser extension is obtained at the top of the first layer, whereby the dose of the layers of the second conducting type will decrease towards the edge of the pn junction.

Another advantage that is achieved with a pn junction structured according to the shown embodiment is that at least one lower doped layer of the second conducting type is situated between a layer of the first conducting type and a higher doped layer of the second conducting type, which relieves a problem with a high electric field being generated within the highly doped layer, when the higher doped layer of the second conducting type directly faces the layer of the first conducting type. The higher doped layer is formed through doping, which may cause damage in the crystal structure of the layer and thereby generate dislocations and as a result exert influence on the electric field conditions locally in the crystal lattice. By means of a lower doped layer as a surplus protection between a higher doped layer of the second conducting type and the boundary layer itself of the junction, a qualitatively better junction is accomplished.

In an alternative method, named B, a JTE for a SiC junction is accomplished by use of a first lower doped layer of the second conducting type closest to the boundary of the pn junction, while the pn junction on the surface of said first layer has a higher doped p-base layer of the second conducting type. The thickness of the first layer is then reduced in a series of etch steps towards the outermost limit of the junction, whereby the total charge content of the volume of each layer step of the first layer will decrease stepwise as a function of the decreasing thickness of the respective layer step.

The field extending efficiency of the JTE produced according to method B is increased with the number of etched down areas. The influence of the number of steps on the field reduction and field uniformity saturates, however, with a high total number of steps. The maximum number of etched down steps is also limited by the costs associated with increasing complexity of the process. One to four etchings steps are realistic and described below.

Another alternative method, method C, to arrive at the JTE according to the invention, comprises combination of etching down, in a number of steps, the lower doped first layer of the second conducting type and ion implantation outside the etched down areas. The ion implantation may be done in one or more steps, where ions, e.g. Boron or Aluminium, are implanted onto the surface of the pn junction layer of the first conducting type just outside the border of the first layer of the second conducting type. The implantation may be effected in regions, outside one another, where the two regions are provided with different charge content. The purpose of the ion implantation is to control the surface doping and the resulting total volume of charge (the resulting volume field at the junction periphery) and the surface field. The last zone can also be created by a vertical epitaxial growth all over the surface.

Finally, an alternative method, D, to perform a Junction Termination Extension of a SiC pn junction is disclosed. The aim is to gradually diminish the doping on the highly doped side of the pn junction (at junction periphery) to secure blocking capability of the high voltage Silicon Carbide component described in the invention. According to method D, the specific SiC technology of lateral growth may be used to apply the basic principles of electric field reduction in the JTE technique. In method D, a JTE at the periphery of the defined pn junction area is accomplished by laterally growing an epitaxial lower doped edge layer of the second conducting type with decreasing doping concentration towards the outermost limit of the junction. The doping concentration may be reduced continuously or in steps. Also a onestep process is available, in that the layer thickness due to the lateral growth technique is decreasing in a direction towards the edge of the junction. Hence the total charge is decreased in the direction from the defined working pn junction area to the outermost edge of the junction. As mentioned, the doping concentration may be varied in steps during the epitaxial growth process of the edge layer. The

doping concentration may as well be continuously controlled during the growth process.

In a somewhat different procedure, D2, the laterally grown layer according to method D is incorporating a thin layer of Aluminium Nitride, AlN, in order to provide a low leakage interface between the vertical part and the lateral part of the edge SiC layer.

For all the described alternatives of a SiC component according to the invention, it is possible to insert an extra low doped (n^{--}) layer of the first conducting type between the lower doped layer (n^{-}) of the first conducting type and the layers of the second conducting type. This may be of importance when the n^{-}-layer has a relatively high doping to arrive at a component of NPT (Non Punch Through) character, whereby the electric field will not reach through the lower doped layers of the first conducting type.

Further small variations of the invention will be illustrated in the embodiments described

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 schematically describes a pn junction according to prior art, where a pn junction with a p-conducting and an n-conducting layer disclose an edge where the p-conducting layer has decreasing dose towards the edge of the pn junction, a so called Junction Termination Extension, JTE.

Figure 2a schematically shows a semiconducting diode of SiC material according to the invention with a voltage absorbing edge, which is edge terminated in that one of the conducting layers of the junction discloses decreasing total charge of the edge towards the edge of the pn junction achieved by epitaxy and etching in more than one step.

Figure 2b shows a variation of the edge terminated junction of figure 2, where a p+ layer is achieved by ion implantation.

Figure 2c shows a variation of the edge terminated junction of figure 2, where an n+ stop is implanted.

Figure 2d shows a semiconductor NPT device of SiC similar to figure 2b, where an extra lower doped layer of the first conducting type is performed at the boundary against layers of the second conducting type.

Figure 3a shows a four step JTE with outwards decreasing charge due to reduced thickness of one of the junction layers at the edge.

Figure 3b shows a two-step JTE of the same type as in figure 3a.

Figure 3c shows a one-step JTE of the same type as in figure 3a.

Figure 4a shows a four step JTE with outwards decreasing charge due to reduced thickness of one of the junction layers and with implanted zones of decreasing total charge at the edge of the junction.

Figure 4b shows a two-step termination corresponding to figure 4a.

Figure 4c shows a one-step termination corresponding to figure 4a.

Figure 4d shows a four-step JTE termination with the fourth zone created by vertical epitaxial growth.

Figure 5a shows the principle of lateral growth of a junction termination layer.

Figure 5b shows a laterally grown layer with stepwise decreasing doping towards the edge of a pn junction.

Figure 5c shows a laterally grown layer with continuously decreasing doping towards the edge of a pn junction.

Figure 5d shows an example of a JTE with an applied laterally grown layer on top of an AlN layer.

DESCRIPTION OF EMBODIMENTS

The invention is described in a number of embodiments with reference to the drawings.

Figure 2a illustrates an example of a pn junction established by the use of method A according to the invention. The pn junction comprises a semiconducting diode manufactured in SiC. When manufacturing a component according to the example, a substrate of SiC consisting of a highly doped (n^+) n-conducting layer 1 is used. On top of this n^+ layer 1, a first lower doped (n^-) n-conducting layer 2 is thereafter epitaxially grown. These two n-conducting layers compose a wafer S of the first conducting type, according to the example n-conducting, on which one or more pn junctions according to the invention can be built. In a second stage a p-conducting low doped second layer 3 is formed on the wafer according to a known technique. In still another stage of the process, outside this second layer, a third highly doped (p^+) p-conducting type layer 4 is grown.

At the next stage the extension of layer 3 i defined by means of masking and etching. In a fourth stage, the third highly doped layer 4 is laterally formed by means of masking and etching to a more limited areal extension than the underlying second layer 3. In this the p-layer on the wafer encloses a decreasing total charge in two steps from the centre of the junction towards the outermost edge 5 of the junction.

Of course, it is possible to epitaxially form more than two layers of the second conducting type on top of each other with the technique that is described in principle in figure 2a, where said layers successively exhibit higher doping concentrations. As a result the charge content of the junction will be decreased laterally towards the edge of the junction, which means that the electric field outwards to the edge becomes more evenly extended. Although, by use of this multi-layer procedure, further process steps arise when manufacturing the component.

Figure 2b depicts an embodiment, where a pn junction is accomplished according to method A2, slighly differing from method A. The layers of the first conducting type, n-layers in the example, are arranged in the same way as in method A, where the wafer S constitutes the base for an epitaxially grown second layer 3 of the second conducting type. This second layer 3 is masked, whereafter a central area of this second layer 3 is implanted with charges of the same type as those in surplus in layer 3, (which in the example means negative charges such as Al or B), whereby a third highly doped layer 8 of the second conducting type is established. An extended edge 5 for the pn junction is generated also in this embodiment of the device by means of etching away the superfluous portion of the second layer 3 of the second conducting type. Otherwise, the component of figure 2b corresponds to what has been described related to that figure, whereby the pn junction according to figure 2b comprises at least one layer with a conducting type which encloses a stepwise decreasing charge towards the edge 5 of the junction.

In the following embodiments, the first conducting type will be represented by n-material, whereas the second conducting type is represented by p-material.

In another alternative embodiment, according to figure 2c, a pn junction is described, produced according to any one of the described embodiments, where a field ring 9, composed of

a n^+-doped region formed as a ring enclosing the edge 5 of the pn junction, is located at a certain distance from the border of the edge 5 according to methods known from corresponding Si technique.

Figure 2a - 2c further shows, as an example, that a semiconductor of SiC is obtained by connection of a cathode 6 to the highly doped n-layer 1 of the wafer, while an anode 7 is connected to the highly doped p-layer 4.

Figures 3a to 3c depict another alternative, referred to as method B above, to achieve a junction termination extension of an SiC pn junction. According to figure 3a a lower doped p layer 10 has been grown epitaxially on top of a wafer S with a surface including a n^--layer 2 as in the previous examples. Also in this alternative the p-layer 10 is covered on its centre portion by a highly doped p^+-layer 11. The inventive concept of this embodiment, i.e. obtaining a diminishing charge content of one layer of the junction towards the edge 5, is arrived at by etching the lower doped p-layer 10 in one or several steps such that the thickness of said p-layer is reduced in steps towards the periphery of the junction. The number of etchings may be chosen according to the required efficiency of distributing the electric field over a larger area. Preferred embodiments are shown in figures 3a to 3c, where in figure 3a four etchings have been carried out. The relation between the thicknesses of the four etched down regions of layer 10, assuming constant doping in the layer 10, is shown in figure 3a as

$$d_0:d_1:d_2:d_3:d_4 = 100:60:45\text{-}50:30\text{-}35:20$$

where d_0 is the relative thickness of the non-etched portion of the defined working area of the junction, whereas d_1 - d_4 are the respective thicknesses of the regions of the etched down areas of the low doped p-layer 10, d_4 being the thickness closest to the edge 5. An estimation of the reduction of the surface field may be calculated from the formula

$$R = \frac{E_{sur_{max}}}{E_{sur_{90°MESA}}} < 10\ \% \qquad (1)$$

where $E_{sur_{max}}$ is the maximum field at the surface of the p-layer 10 in regions d_1 - d_4 and $E_{sur_{90°MESA}}$ the field existing at a MESA edge with a p-layer terminated by a 90 degree edge where no JTE had been formed.

Further, simpler embodiments of method B are disclosed in figures 3b and 3c, where in figure 3b a two step junction termination is shown, the ratio between the thicknesses of the unetched and the two etched edge regions being $d_0:d_1:d_2$ = 100:60:30-35. Figure 3 shows in turn a one-step junction termination, with the corresponding relation between the thicknesses being $d_0:d_1$ = 100:50 - 60. The surface field reduction achieved may be estimated by the quotient R according to formula (1) being less than 20 % for a device of figure 3b and less than 50 % for a device of figure 3c.

A surface passivation layer L1 is also illustrated in figures 3a - 3c.

Still another alternative, method C, to produce a termination according to the invention is described and suported by figures 4a - 4d. This method resembles method B, in that the lower doped p-layer 12 is etched down in at least one step in order to give each region of a prescribed amount of total charge content, as was also the case of method B. In method C at least one region of the n^--layer 2 of the wafer S outside the border of the p-layer 12 is implanted with negative charges (e.g. Boron of Aluminium ions) to provide the surface of the n^--layer 2 with a thin layer of p-type material. As is shown in figure 4a, the symbol Q_3 denote the total amount of negative charge in the region. The embodiment of figure 4a depicts a four-step junction termination, where the junction is terminated by two etched down regions Q_1 and Q_2 and outside the end of the

p-layer 12 two implanted p-regions Q_3 and Q_4, respectively. The total charge content of the respective region is given by the relation

$$Q_0:Q_1:Q_2:Q_3:Q_4 = 100:60:45\text{-}50:33:20$$

where Q_0 represents the total charge of the full depth region of the p-layer 12. The surface field reduction obtained according to formula 1 is calculated to be $R < 10$ %.

Corresponding edge terminations are shown in figures 4b and 4c, where in figure 4b a two-step termination is illustrated showing one etched down step Q_5 of p-layer 12 and an implanted p-region Q_6 of the n-layer 2. In the same way a termination according to figure 4c is arrived at by a complete etching of the p-layer 12 outside the p^+-layer 13 on top of the defined working area of the junction, whereafter a p-layer Q7 of a preferred amount of total charge is implanted outside and at the border of the p-layer 12. In figure 4d a four-step JTE termination with the fourth zone created by vertical epitaxial growth is shown.

Method D is finally described with reference to figures 5a - 5d. By growing epitaxially a p^--layer 17 laterally on a pn junction mesa consisting of a n^--layer 15 on a wafer S and a p^+-layer 16 formed on the wafer, the epitaxially grown layer 17 will adapt the form as shown in principle in figure 5a. The thickness of the lateral layer 17 decreases in a direction from the mesa edge towards the outer border of the lateral layer 17. It has been experimentally verified when epitaxially growing a layer on a mesa edge, that the grown layer will assume the laterally extended form illustrated in figure 5a. Due to the reduction of thickness of the laterally formed layer 17, said layer will have by itself the property of distributing the field of the edge termination T constituted by layer 17.

By using the principle described of lateral growing of a p^--layer 17, where the lateral growth is performed in successive operations with a lowering of the doping in each

operation, a junction termination according to figure 5b is obtained. A multistep JTE, where the p^+ base layer 16 is surrounded by successively grown p-type layers with gradually lower dopings is then established. The successive growth of lower doped layers may involve intermediate etch-back operations or both etch-back and patterning operations to optimise the resulting p-type doping profile of the JTE.

A similar principle is used in figure 5c, where the laterally grown layer 17 is afforded a gradually decreased doping concentration outwards by continuous reduction of the dose of the doping gas during the epitaxial lateral growth of said layer 17. The arrow 18 shows the direction of diminishing doping concentration.

In figure 5d an embodiment showing a layer 19 of AlN covering an etched mesa of the junction is illustrated. The AlN is grown using the same epitaxial technique as is used for lateral growth of SiC. The AlN-layer 19 is built before the laterally grown layer 17 is applied to the junction edge. The AlN-layer 19 is incorporated in order to provide a low leakage interface between the vertically and laterally portions of the mesa. The low leakage interface obtained by inserting a layer of AlN in the form of layer 19 may also be achieved in the embodiments shown in figures 5b and 5c.

The doping concentrations above referred to as symbols can be deduced from the suggestions in the table below.

p^+	10^{18}	-	10^{21} cm^{-3}
p	10^{15}	-	$5 \cdot 10^{17}$ cm^{-3}
n^-	10^{14}	-	10^{16} cm^{-3}
n^+	10^{15}	-	10^{21} cm^{-3}

CLAIMS

1. A semiconductor component comprising a pn junction, where both a first conducting type (n) layer and a second conducting type (p) layer of the pn junction constitute doped layers of silicon carbide (SiC), the edge of at least one of said layers being provided with an edge termination (T), **characterized in** that the edge termination (T) encloses stepwise or continuously decreasing total charge towards the outer border of the termination.

2. Semiconductor component according to claim 1, **characterized in** that the pn junction comprises a first lower doped layer (3) of the second conducting type and a second higher doped layer (4, 8) of the second conducting type on top of said first layer, the second layer (4, 8) having a smaller areal extension than said first layer (3).

3. Semiconductor component according to claim 1, **characterized in** that the pn junction comprises a first lower doped layer (10) of the second conducting type and a second higher doped layer (11) of the second conducting type on top of said first layer, the first layer (10) having at its periphery its thickness reduced to zero in steps (d_0 - d_4).

4. Semiconductor component according to claim 1, **characterized in** that the pn junction comprises a first lower doped layer (12) of the second conducting type, a second higher doped layer (13) of the second conducting type on top of said first layer, the first layer (12) outside the border of the second layer (13) having at its periphery its thickness reduced to zero in steps (Q_0, Q_1, Q_2, Q_5) and outside and adjacing said first layer (12) at least one implanted first layer surrounding zone (Q_3, Q_4, Q_6, Q_7) of the second conducting type, whereby the steps of the first layer (12) and the implanted zones (Q_3, Q_4, Q_6, Q_7) constitute the termination (T).

5. Semiconductor component according to claim 1, **characterized in** that the second conducting type layer of the pn junction comprises a first higher doped layer (16) surrounded by a second conducting type edge laterally formed layer (17) with outwards stepwise or continuously decreasing doping concentration forming the termination (T).

6. Semiconductor component according to claim 5, **characterized in** that an AlN layer is applied between the laterally grown edge layer (17) and the rest of the SiC component.

7. Semiconductor component according to any of the preceding claims, **characterized in** that an extra doped layer (21) is applied between the lower doped layer (2) of the first conducting type and the layers of the second conducting type of the junction, the extra layer (21) being of the first conducting type (n^{--}) and having a lower doping concentration than the lower doped (n^-) layer (2) of the first conducting type.

8. Method of manufacturing a semiconductor component comprising a pn junction, where both the p-conducting and the n-conducting layers of the pn junction constitute doped layers of silicon carbide (SiC), the edge of at least one of the layers provided with an edge termination (T), **characterized in** that on a silicon carbon wafer (S) comprising a doped layer (2) of a first conducting type at least two doped layers (3, 4), (3, 8) of a second conducting type are arranged on top of each other, the doping concentration of each new second conducting type layer being successively increased, the layers of the second conducting type then being formed to have successively reduced areas, in that a termination (T) of the layers of the second conducting type provided with decreasing total charge or decreasing charge density per unit area towards the edge (5) is established.

9. Method according to claim 8, **characterized in** that the layers (3, 4) of the second conducting type are grown epitaxially on top of each other.

10. Method according to claim 9, **characterized in** that the layers (3, 4) of the second conducting type by means of masking are etched down in steps, in that the successive layers are provided with successively reduced areas.

11. Method according to claim 8, **characterized in** that the layers (3, 8) of the second conducting type are formed by implantation of ions on top of at least one first epitaxial grown layer (3), thereby forming a second layer (8) with a higher doping concentration than the underlying layer (3).

12. Method according to claim 11, **characterized in** that the epitaxially grown layers (3) of the second conducting type lying below the implanted layer (8) are etched down in steps by means of masking, in that the successive layers of the second conducting type (3, 8) are provided with successively reduced areas.

13. Method of manufacturing a semiconductor component comprising a pn junction, where both the p-conducting and the n-conducting layers of the pn junction constitute doped layers of silicon carbide (SiC), the edge of at least one of the layers being provided with an edge termination (T), **characterized in** that on a silicon carbon wafer (S) comprising a doped layer (2) of a first conducting type at least a first lower doped layer (10) of a second conducting type is epitaxially grown, on top of this first layer (10) a second higher doped layer (10) of the second conducting type being epitaxially grown, the first layer (10) outside the outer border of the second layer (11) then, by means of masking and etching in steps, being formed to have stepwise reduced thickness (d_0 - d_4) towards the periphery of said first layer (10), in that a termination (T) of the layers of the second conducting type provided

with decreasing total charge towards the edge (5) is established.

14. Method according to claim 13, **characterized in** that the relative thicknesses of the steps of a four-step first layer (10) of the second conducting type is $d_0:d_1:d_2:d_3:d_4$ = 100:60:45-50:30-35:20, the relative thicknesses of the steps of a two-step first layer (10) of the second conducting type is $d_0:d_1:d_2$ = 100:60:30-35 and the relative thicknesses of the steps of a one-step first layer (10) of the second conducting type is $d_0:d_1$ = 100:50 - 60.

15. Method of manufacturing a semiconductor component comprising a pn junction, where both the p-conducting and the n-conducting layers of the pn junction constitute doped layers of silicon carbide (SiC), the edge of at least one of the layers being provided with an edge termination (T), **characterized in** that on a silicon carbon wafer (S) comprising a doped layer (2) of a first conducting type at least a first lower doped layer (12) of a second conducting type being epitaxially grown, on top of this first layer (12) a second higher doped layer (13) of the second conducting type is epitaxially grown, the first layer (12) outside the outer border of the second layer (13) then by means of masking and etching in steps being formed to have stepwise reduced thickness (Q_0, Q_1, Q_2, Q_5) towards the periphery of said first layer (12) and that outside and adjoining the border of said first layer (12) of the second conducting type at least one first layer surrounding zone (Q_3, Q_4, Q_6, Q_7) with decreasing total charge towards the edge (5) is implanted with ions of the second conducting type on top of the wafer (S), in that a termination (T) of the layers of the second conducting type provided with decreasing total charge towards the edge (5) is established.

16. Method according to claim 15, **characterized in** that the relation between charges of a four-step reduced charge at the termination (T) comprising layers (10, Q_3, Q_4) of the

second conducting type is $Q_0:Q_1:Q_2:Q_3:Q_4$ = 100:60:45-50:30-35:20.

17. Method according to claim 15, **characterized in** that the implantation is performed with boron or aluminium ions.

18. Method of manufacturing a semiconductor component comprising a pn junction, where both the p-conducting and the n-conducting layers of the pn junction constitute doped layers of silicon carbide (SiC), the edge of at least one of the layers being provided with an edge termination (T), **characterized in** that on a silicon carbon wafer (S) comprising a doped layer (2) of a first conducting type a first high doped layer (16) of a second conducting type is epitaxially grown, a junction edge then being formed by etching said first layer (16) and said doped layer (2) of the first conducting type to a mesa structure, an edge layer (17) then being laterally grown at the edge of the junction with stepwise or continuously decreasing doping concentration outwards, thereby forming a termination (T) of the layer of the second conducting type with decreasing total charge towards the edge (5).

19. Method according to claim 18, **characterized in** that the edge layer (17) is grown by means of intermediate etch-back operations.

20. Method according to claim 18, **characterized in** that the reduction of the doping concentration of the edge termination (T) is achieved by continuous or stepwise reduction of the dose of a doping gas during the epitaxial growth of the edge layer (17).

21. Method according to any of claims 13, 19 or 20, **characterized in** that a layer (18) of AlN is formed (*epitaxially*) on the mesa structure before growing an edge layer (17) on top of said AlN layer (18).

22. Method of manufacturing a semiconductor component comprising a pn junction, where both the p-conducting and the n-conducting layers of the pn junction constitute doped layers of silicon carbide (SiC), the edge of at least one of the layers being provided with an edge termination (T), **characterized in** that on a silicon carbon wafer (S) comprising a doped layer (2) of a first conducting type at least a first lower doped layer (12) of a second conducting type is epitaxially grown, on top of this first layer (12) a second higher doped layer (13) of the second conducting type being epitaxially grown, the first layer (12) outside the outer border of the second layer (13) then, by means of masking and etching in steps, being formed to have stepwise reduced thickness towards the periphery of said first layer (12) and outside said steps at least one zone of a material with the lowest total charge is created by vertical epitaxial growth, in that a termination (T) of the layers of the second conducting type provided with decreasing total charge towards the edge (5) is established.

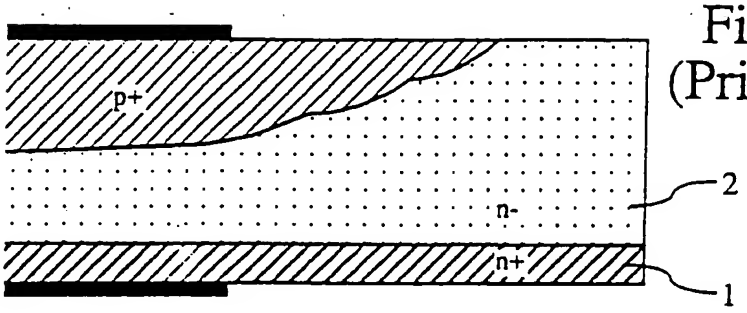


Fig. 1
(Prior art)

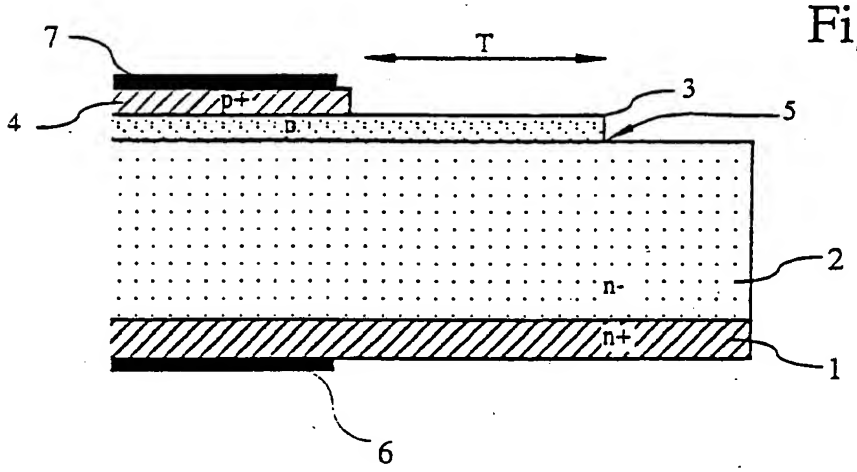


Fig. 2a

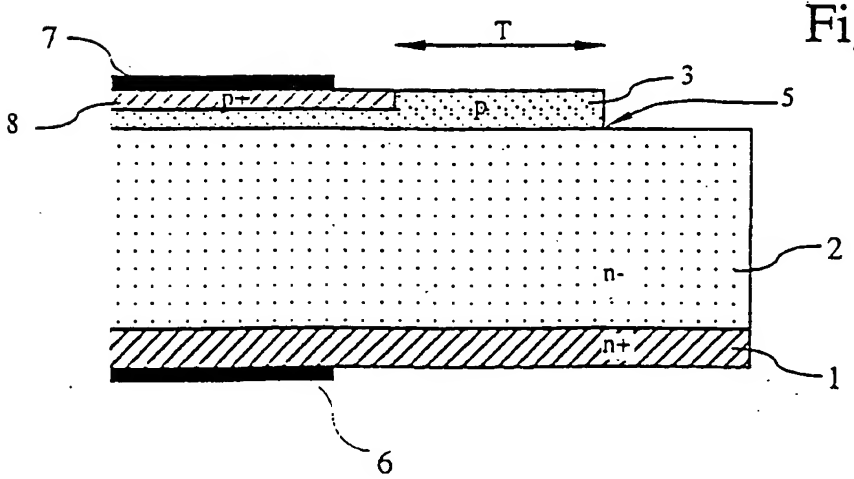


Fig. 2b

Fig. 2c

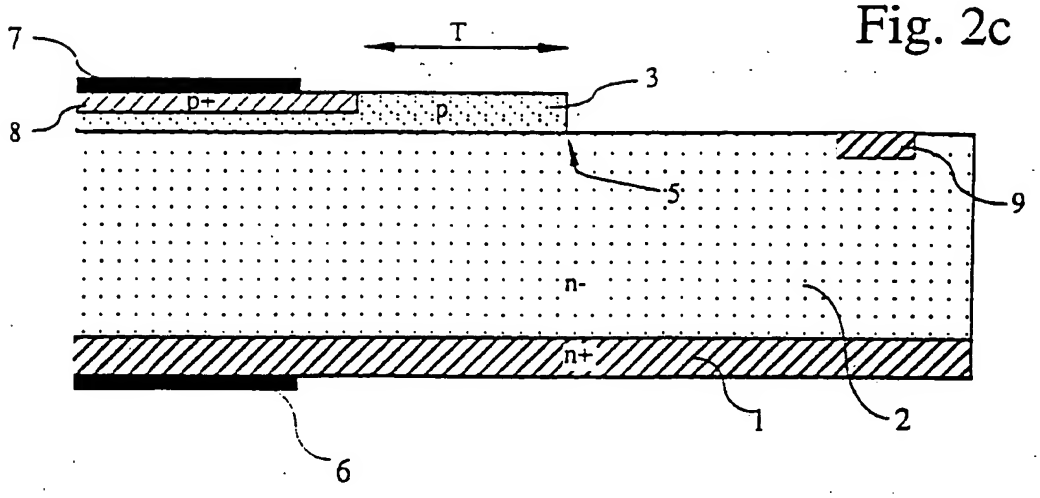


Fig. 3a

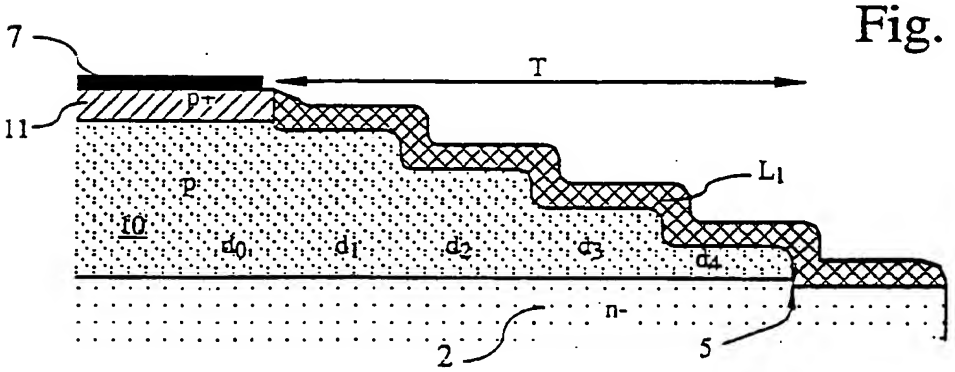
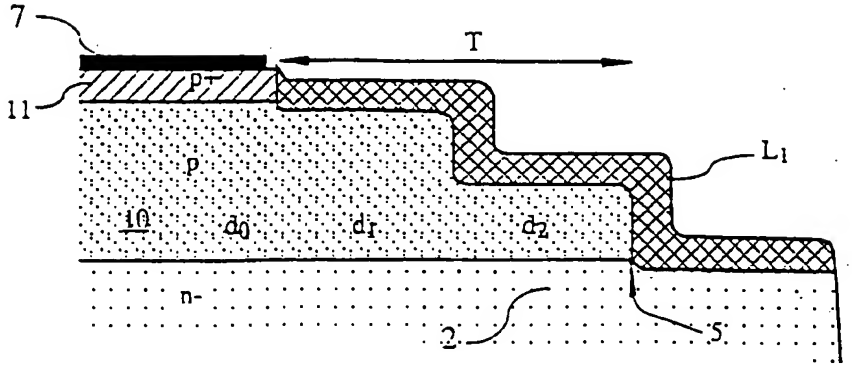


Fig. 3b



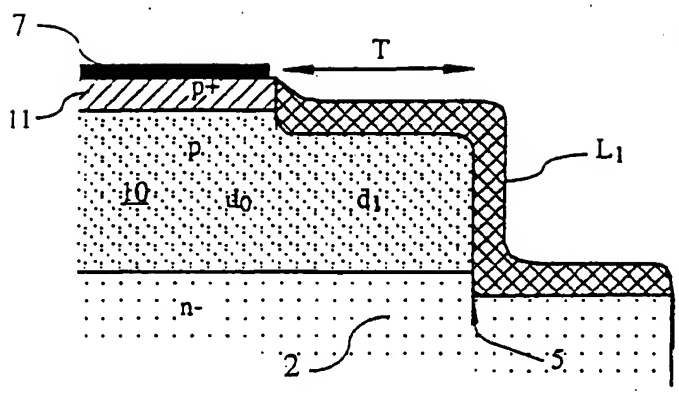


Fig. 3c

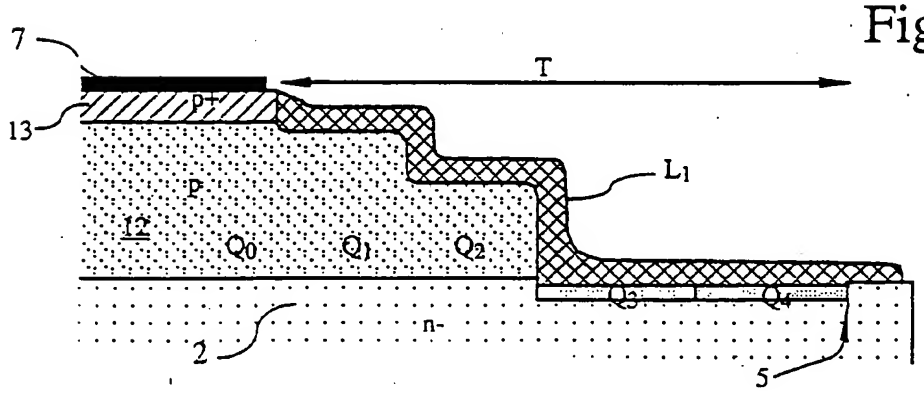


Fig. 4a

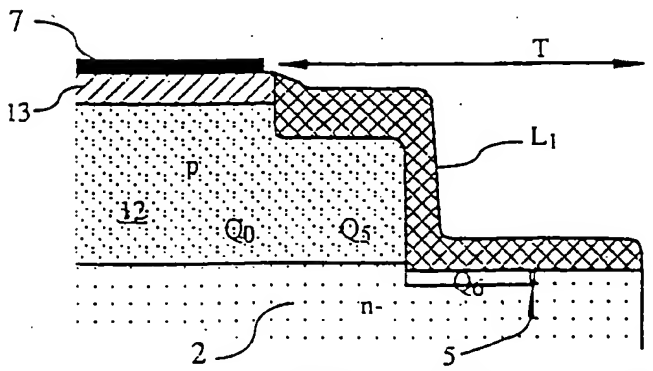


Fig. 4b

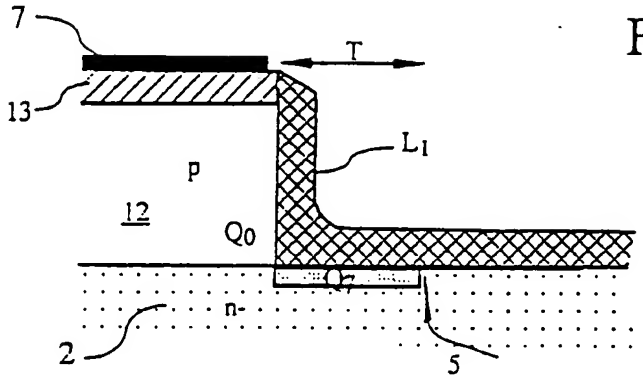


Fig. 4c

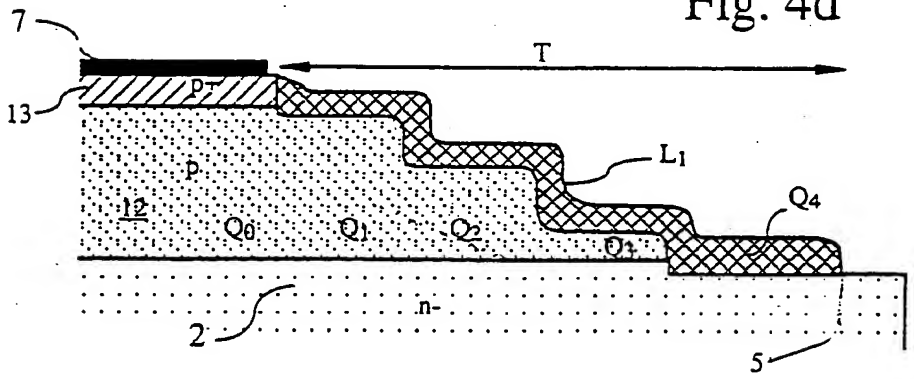


Fig. 4d

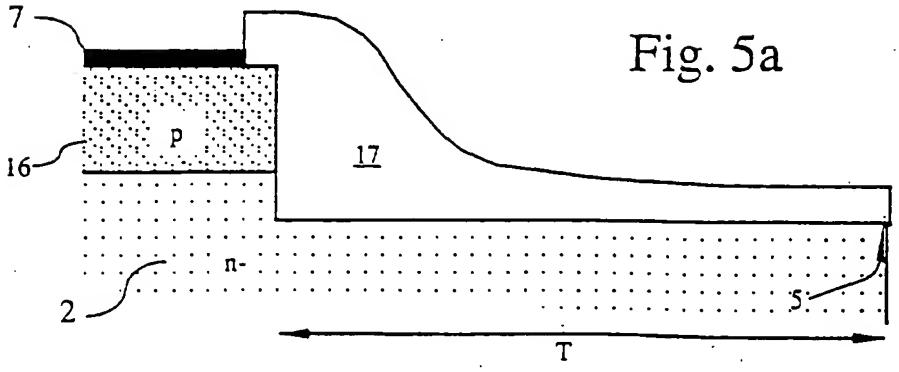


Fig. 5a

Fig. 5b

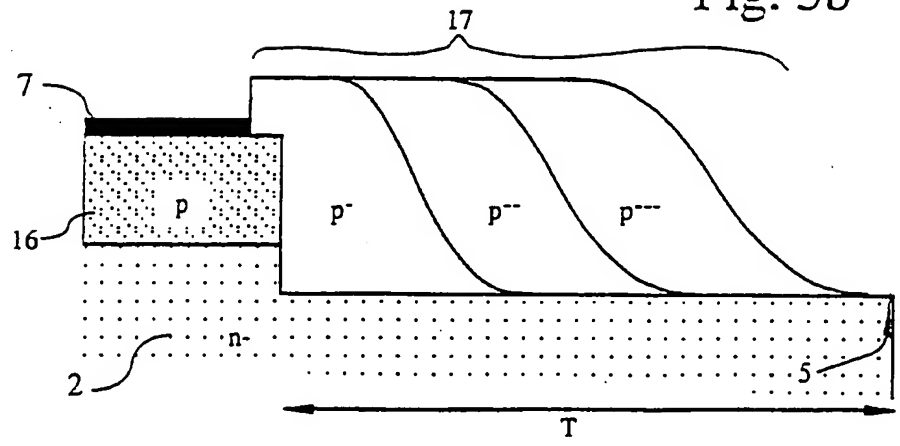


Fig. 5c

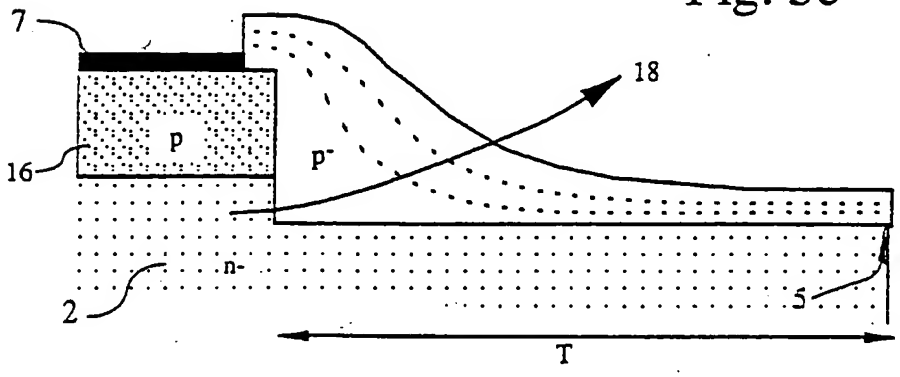


Fig. 5d